What is Claimed is:

1. A method for correcting distortions in a signal that includes logical data comprising:

receiving said signal;

comparing a portion of said signal to a signal-eye;

determining said logical data based upon said comparing;

determining said timing distortions of said portion; and

centering said signal-eye with respect to said portion based upon said determined timing distortions.

2. The method of claim 1 wherein said comparing comprises comparing a voltage threshold to said portion.

3. The method of claim 2 wherein said centering said signal-eye comprises adjusting said voltage threshold.

4. The method of claim 1 wherein said comparing further comprises comparing a current threshold to said portion.

5. The method of claim 4 wherein said centering said signal-eye comprises adjusting said current threshold.

6. The method of claim 1 wherein said centering said signal-eye comprises adjusting the voltage of said portion.

7. The method of claim 6 wherein said adjusting the voltage of said portion comprises sinking the current of said portion.

8. The method of claim 1 wherein said centering said signal-eye comprises adjusting the current of said portion.

9. The method of claim 1 wherein said portion is a bit of said logical data is defined by a positive signal component and a negative signal component and an average of said positive signal component and negative signal is compared to said signal-eye.

10. The method of claim 1 wherein said determining said distortions comprises performing a bit-error-rate analysis on said signal.

11. The method of claim 1 wherein said determining said distortions comprises comparing a peak voltage for said portion to an ideal peak voltage for said portion.

12. A system for correcting an asymmetrical signal with respect to a signal-eye comprising:

a communication channel providing said signal;

a clock and data recovery decision circuit, coupled to said communication channel, for determining the logical data included in said signal, wherein said signal-eye is compared to an average value of said signal; and

a threshold adjust block, coupled to said communication channel, for providing symmetry between said signal and said signal-eye.

13. The system of claim 12, wherein said signal-eye is a voltage threshold.

14. The system of claim 13, wherein said threshold adjust block adjusts said voltage threshold.

15. The system of claim 12, wherein said signal-eye is a current threshold.

16. The system of claim 15, wherein said threshold adjust block adjusts said current threshold.

17. The system of claim 12, wherein said threshold adjust block adjusts the voltage of said signal on said communication channel.

18. The system of claim 17, wherein said threshold adjust block decreases the voltage of said signal on said communication channel.

19. The system of claim 18, wherein said threshold adjust block decreases the voltage of said signal by sinking current from said communication channel.

20. The system of claim 12 further comprising a distorted signal detector coupled to said communications channel for detecting distortions in said signal.

21. The system of claim 20 wherein said distorted signal detector performs a bit-error-rate

analysis of said logical data to detect said distortions.

22. The system of claim 20, wherein said distorted signal detector compares a peak voltage of said signal to an ideal peak voltage for said signal to detect said distortions.

23. The system of claim 20, wherein said distorted signal detector is coupled to said threshold adjust block and controls the operation of said threshold adjust block.

24. The system of claim 12, further comprising a programmable logic device coupled to said clock and data recovery circuit wherein said programmable logic device receives the logical data included in said signal.

25. A system for correcting an asymmetrical signal with respect to a signal-eye comprising:

a communication channel providing said signal; and

a threshold adjust block, coupled to said communication channel, for providing symmetry between said signal and said signal-eye, wherein said threshold adjust block adjusts said signal-eye by adjusting the amount of current in said signal.

26. The system of claim 25 wherein said threshold adjust block sinks current from said signal.

27. The system of claim 25 further comprising: a clock and data recovery decision circuit, coupled to said communication channel, for determining

the logical data included in said signal, wherein said signal-eye is compared to an average value of said signal.

28. The system of claim 27 further comprising a programmable logic device coupled to said clock and data recovery circuit, wherein said programmable logic device receives the logical data included in said signal.

29. The system of claim 25 wherein said threshold adjust block is operable to adjust the current of said signal at a plurality of current amounts.

30. The system of claim 29 further comprising a plurality of control signals having a plurality of logical combinations, wherein at least one of said plurality of logical combinations sinks current from said signal by one of said plurality of current amounts.

31. The system of claim 29 further comprising a plurality of control signals having a plurality of logical combinations, wherein at least one of said plurality of logical combinations increases current from said signal by one of said plurality of current amounts.

32. The system of claim 29 further comprising a control signal that determines if the amount of current in said signal is increased or decreased.